START UP CIRCUIT FOR DELAY LOCKED LOOP

ABSTRACT OF THE DISCLOSURE

An initialization circuit in a delay locked loop ensures that after power up or other reset clock edges are received by a phase detector in the appropriate order for proper operation. After reset of the delay locked loop, the initialization circuit assures that at least one edge of a reference clock is received prior to enabling the phase detector to increase (or decrease) the delay in a delay line. After at least one edge of a feedback clock is received, the initialization circuit enables the phase detector to decrease (or increase) the delay in a delay line.